

## Low Voltage Wide Ratio Current Mirror

### Field of the Invention

[0001] The invention relates to the field of current mirror circuits and more specifically to the field of current mirror circuits for operating at low voltages.

### Background of the Invention

[0002] Current sources made by using active devices have come to be widely used in analog integrated circuits for both biasing elements as well as load devices for amplifier stages. The use of current sources in biasing can result in superior insensitivity of circuit performance to power supply variations and to temperature. When used as a load element in transistor amplifiers, the high incremental resistance of the current source results in high voltage gain at low power-supply voltages.

[0003] Current mirror circuits are typically used for generating an accurate large current from a small reference current. Current mirror circuits that operate at low supply voltages must be able to generate the accurate larger current when the supply voltage is less than twice a base emitter voltage drop ( $V_{be}$ ) for a bipolar transistor or when the supply voltage is less than twice a threshold voltage ( $V_t$ ) for a FET device. These low supply voltages can occur in devices that operate using two 0.9V battery cells, such as mobile terminals.

[0004] A prior art patent, EP 1 213 636 describes a current mirror circuit. Unfortunately, this circuit does not allow wide ratio operation and is more difficult to stabilize. The current ratio is limited to the ratio of the NPN devices used. Loop stability is harder to achieve since it is difficult to achieve one dominant loop pole. Stability in the current mirror is known to those of skill in the art to be an important quality for the current mirror circuit because of the potential to introduce oscillations that disrupt the operation of the load circuit. Wide ratio current mirrors are often used with power amplifier circuits and the wide ratios required by these PAs are not attainable by other means. Utilizing a low ratio current mirror would result in appreciable wasted current

consumption by virtue of the fact that the bias circuits would have to provide much greater input currents. In other words, the current being ‘mirrored’ becomes a more significant fraction of the current being supplied to the load. When the mirror output transistor is modulated with a large amplitude RF signal another disadvantage of this scheme becomes apparent, particularly where a large mirror ratio is chosen. The RF signal causes an increase in the mean collector current in the modulated transistor and therefore an increase in the mean base current. This is because the transistor is biased into class B operation. This mean base current is sourced from the current mirror not from the RF source and is usually significantly larger than the quiescent component. Thus a large RF signal can reduce the effective mirror ratio.

**[0005]** Other solutions that incorporate operational amplifiers (OpAmps) are also known to those of skill in the art, however these circuits are quite complex and often less accurate. An Opamp, on its own, is inherently more complex than simple transistor circuits. Opamp circuits are subject to voltage offset, which can be an issue when we are dealing with NPN current mirror circuits where a few mV represents a significant error term. They typically are not able to operate at 1.5V. Other conventional current mirror circuits also have difficulties operating with large ratios.

**[0006]** A need therefore exists for a wide ratio current mirror for offering stable operation at low supply voltages. It is therefore an object of the invention to provide a wide ratio and low voltage current mirror that offers stability at low supply voltages. It is a further object of the invention to provide low voltage current mirror for use with a differential amplification stage.

### **Summary of the Invention**

**[0007]** In accordance with the invention there is provided a circuit comprising: a first supply voltage port; a second supply voltage port; a current mirror circuit comprising a first current mirror port and a second current mirror port, the second current mirror port for propagating an input current from the first supply voltage port to the second supply port through the current mirror circuit coupled therebetween, where the first current

mirror port is for providing  $N$  times the input current; and, a current ratioing circuit comprising a first portion disposed between the first current mirror port and the second supply voltage port and a second portion disposed between the first supply voltage port and the second supply voltage port, the second portion comprising a load current path, where the current ratioing circuit is for propagating  $M$  times  $N$  times the input current through the load current path.

**[0008]** In accordance with the invention there is provided a method comprising: providing a current mirror circuit having a first mirror portion and a second mirror portion, the first portion for propagating  $N$  times more current than the second portion; providing a current ratioing circuit having a first portion and second portion, the second portion for propagating  $M$  times more current than the first portion; propagating of an input current through a second portion of the current mirror circuit; mirroring of the input current in the first portion to provide  $N$  times the input current; receiving of the  $N$  times the input current by the current ratioing circuit; and, ratioing of the  $N$  times the input current so that  $N$  times the input current propagates through the first portion and  $M$  times  $N$  times the input current propagates through the second portion.

#### **Brief Description of the Drawings**

**[0009]** Exemplary embodiments of the invention will now be described in conjunction with the following drawings, in which:

**[0010]** FIG. 1 illustrates a prior art current mirror circuit;

**[0011]** FIG. 2 illustrates a schematic of a wide ratio current mirror circuit in accordance with a first embodiment of the invention;

**[0012]** FIG. 3 illustrates an implementation of a wide ratio current mirror circuit, in accordance with a second embodiment of the invention, for use with a power amplifier (PA) stage; and,

**[0013]** FIGs. 4a and 4b illustrates an implementation of a variation of the wide ratio current mirror circuit for use with a differential RF input signal, in accordance with third and fourth embodiments of the invention.

### **Detailed Description of Embodiments of the Invention**

**[0014]** Referring to prior art FIG. 1, disclosed in EP 1,213,636, a current mirror circuit 100 is shown comprising two bipolar transistors 10 and 12 as well as the current source 14 for providing a reference current ( $I_r$ ). An output current ( $I_a$ ) for being generated by the current mirror circuit 100 propagates through load resistor R 22.

**[0015]** The current mirror circuit 100 comprises a further current mirror circuit that includes two p-channel MOS field-effect transistors 16 and 18 as well as an n-channel MOS field-effect transistor 20 that receives  $I_r$  from the current source 14 through its gate terminal. Gate terminals of the p-channel MOS field-effect transistors 16 and 18 are connected to each other and their source terminals are connected to a positive supply voltage port for receiving the supply voltage VDD. The drain of the p-channel MOS field-effect transistor 16 is connected to the gate terminals of these two MOS transistors 16 and 18. Furthermore, the drain of the p-channel MOS field-effect transistor 16 is connected to the drain of the n-channel MOS field-effect transistor 20, with a source terminal thereof directly connected to ground. The potential on the gate terminal of NFET 20 rises until sufficient current flows in the base of NPN transistor 10 to allow the collector current of NPN transistor 10 to match the current from the current source 14. Since NFET 20 draws no gate current this match is exact – independent of the current being drawn by the base of NPN 12.

**[0016]** Furthermore, the current mirror circuit of prior art FIG. 1 does not allow wide ratio operation and is more difficult to make stable. The current ratio is limited to the ratio of the NPN devices used. A practical limit to the ratio is perhaps 20 to 40 times a maximum current ratio in order to attain proper matching. Stability is harder to achieve since it is difficult to achieve one dominant loop pole.

**[0017]** FIG. 2 illustrates a schematic of a wide ratio current mirror circuit 200 in accordance with a first embodiment of the invention. The wide ratio current mirror circuit 200 comprises a first FET M1, a second FET M2, a third FET M3, a current sink 221 for sinking current  $I_{in}$ , a first bipolar transistor Q1 201, a second bipolar transistor Q2 202

and a load resistor R1 231. A first supply voltage port 200a is used for providing a positive supply voltage to the wide ratio current mirror circuit 200 and a second supply voltage port 200b is used for providing a negative, or ground, supply voltage to the wide ratio current mirror circuit 200.

**[0018]** A current mirror circuit 205 is formed from first and second transistors in the form of p channel FETs M1 211 and M2 212, respectively, which are coupled with their source terminals to the first supply voltage port 200a. The gate terminals of the p channel FETs M1 211 and M2 212 are coupled together, coupled to the drain terminal of FET M1 211, and further coupled to the first current mirror port 205b. A second current mirror port 205a is formed at the drain terminal of FET M2 212. FETs M1 211 and M2 212 are formed so as to provide a statistical match with a current ratio of N times. The current in the drain terminal of FET M1 211 is N times the current in the drain terminal of FET M2 212, which functions as a current reduction circuit.

**[0019]** Transistors Q1 201 and Q2 202 form a current ratioing circuit 206 circuit that includes a first portion disposed between the first current mirror port 205b and the second supply voltage port 200b and a second portion disposed between the first supply voltage port 200a and the second supply voltage port 200b, the second portion including a load current path that includes a load resistor 231. A current path is formed between the first supply voltage port 200a and the coupled base terminals of transistors Q1 201 and Q2 202. The current path includes a FET M3 213, with source and drain terminals disposed in series with the current path from the first supply voltage port 200a to coupled base terminals of transistors Q1 201 and Q2 202. The gate terminal of FET M3 213 is coupled with the second current mirror port 205a. Transistors Q1 201 and Q2 202 are formed so as to provide a statistical match with M times current ratio. The current flowing in the collector terminal of transistor Q2 202 is M times the current flowing in the collector terminal of transistor Q1 201. For the load current path, resistor R1 231 is disposed between the current ratio output port 206b and the first supply voltage port 200a.

**[0020]** In equilibrium the drain current of FET M2 212 exactly balances the current  $I_{in}$  sunked through the current sink 221 and the potential on the drain terminal of FET M2 212 biases the gate terminal of FET M3 213. This causes current flow in the drain terminal of FET M3 213, which drives the base terminals of transistors Q1 201 and Q2 202. The resultant collector current in transistor Q1 201 drives the first current mirror port 205b and causes current to flow in the drain terminal of FET M2 212. By making FET M1 211 N times wider than FET M2 212 the current flowing in the collector terminal of Q1 201 is N times larger than the current flowing in the drain terminal of FET M2 212. By making transistor Q2 202 M times larger than transistor Q1 201 the current flowing in the collector terminal of Q2 202 is M times larger than the current flowing in the collector terminal of transistor Q1 201. Thus, the current propagating through the load resistor,  $R_1$ , is  $M^*N^*I_{in}$ . Advantageously, FET devices, M1 211 and M2 212, have longer channels and have sufficient gate area to provide the statistical match, whereas FET M3 312 is a short channel device.

**[0021]** Just as in the prior art, the limit on the ratio M of the two bipolar transistors Q1 201 and Q2 202 is about 20 or 40 to one. However by use of the FET mirror of M1 211 and M2 212 the overall current gain of the circuit is extended by N times.

**[0022]** FIG. 3 illustrates an implementation of a wide ratio current mirror circuit 300, in accordance with a second embodiment of the invention, for use in receiving of an RF input signal through a RF signal input port 300c. The wide ratio current mirror circuit 300 comprises a first transistor, in the form of a first FET M1 311, a second transistor, in the form of a second FET M2 312, a fifth transistor, in the form of a third FET M3 313, a first current sink 321 for sinking current  $I_{in}$ , a third transistor, in the form of a first bipolar transistor Q1 301, a fourth transistor, in the form of a second bipolar transistor Q2 302, a load resistor  $R_1$  331, resistors R2 332 R3 333 R4 334, and capacitors C2 342 C1 341. A first supply voltage port 300a is used for providing a positive supply voltage to the wide ratio current mirror circuit 300 and a second supply voltage port 300b is used for providing a negative, or ground, supply voltage to the wide ratio current mirror circuit 300.

[0023] A current mirror 305 is formed from FETs M1 311 and M2 312. The source terminals of the p channel FETs M1 311 and M2 312 are coupled to the first supply voltage port 300a. The gate terminals of the p channel FETs M1 311 and M2 312 are coupled together, coupled to the drain terminal of FET M1 311, and further coupled to the collector terminal of transistor Q1 301. A source terminal of FET M3 313 is coupled to the first supply voltage port 300a, with the gate terminal thereof coupled to the drain terminal of FET M2 312. A first current mirror port 305a is formed at the drain terminal of FET M2 312 and a second current mirror port 305b is formed at the drain terminal of FET M1 311.

[0024] Transistors Q1 301 and Q2 302 form a current ratioing circuit 306 circuit that includes a first portion disposed between the first current mirror port 305b and the second supply voltage port 300b and a second portion disposed between the first supply voltage port 300a and the second supply voltage port 300b, the second portion including a load current path that includes a load resistor 331. A current path is formed between the first supply voltage port 300a and the coupled base terminals of transistors Q1 301 and Q2 302. The current path includes the FET M3 313 and resistor R2 332 with source and drain terminals disposed in series with resistor R2 332 from the first supply voltage port 300a to coupled base terminals of transistors Q1 301 and Q2 302. The gate terminal of FET M3 313 is coupled with the second current mirror port 305a. Transistors Q1 301 and Q2 302 are formed so as to provide a statistical match with M times current ratio. The current flowing in the collector terminal of transistor Q2 302 is M times the current flowing in the collector terminal of transistor Q1 301. For the load current path, resistor R1 331 is disposed between the current ratio output port 306b and the first supply voltage port 300a. The base terminal of transistor Q1 301 is coupled with the base terminal of transistor Q2 302 through resistors R3 333 and R4 334 in series. A node is formed between resistors R3 333 and R4 334 is coupled with resistor R2 332 to the drain terminal of FET M3 313. The current sink 321 for sinking current  $I_{in}$  is disposed between the second supply voltage port 300b and the gate and drain terminals of FET M2 312 and the gate terminal of FET M3 313, respectively.

[0025] A capacitor C1 341 is disposed between the gate and drain terminals of FET M3 313. Capacitor C2 342 is disposed between the RF input port 300c and the base terminal of transistor Q2 302 for capacitively coupling of the RF input signal thereto, where transistor Q2 302 is modulated through capacitor C2 342 by the RF input signal. Resistor R4 334 provides a DC potential to the base terminal of transistor Q2 302, where resistor R3 333 provides a similar DC potential to the base terminal of transistor Q1 301. Capacitor C1 341 provides loop stabilization for FET M3 313 and resistor R2 332 aids in a pole split for the wide ratio current mirror circuit 300. Resistor R2 332 is used to isolate FET M3 313 from the resistively coupled base terminals of transistors Q1 301 and Q2 302. A voltage drop across resistor R3 333 matches the voltage drop across resistor R4 334.

[0026] Miller feedback within the circuit is a result of the dominant pole formed by FET M3 313. A small change in current of FET M3 reflects back to gate terminal through capacitor C1 341, where resistor R2 332 and capacitor C1 341 operate in conjunction as a voltage swing reduction circuit to reduce large voltage swings on the gate terminal of FET M3 313. Opposite to that which is provided by the prior art illustrated in FIG. 1a, which provides no stabilization correction.

[0027] In equilibrium, the drain current of FET M2 312 balances the current I<sub>in</sub> sunked from the current sink 321 and the potential on the drain of FET M2 312 biases the gate terminal of FET M3 313. This causes current flow in the drain terminal of FET M3 313, which drives the base terminals of transistors Q1 301 and Q2 302. The resultant collector terminal current in transistor Q1 301 drives the first current mirror port 305b, through the first current ratio port 306a, and causes current to flow in the drain terminal of FET M2 312. By making FET M1 311 N times wider than FET M2 312 the current in the collector terminal of transistor Q1 301 is N times larger than the current in the drain terminal of FET M2 312. By making transistor Q2 302 M times larger than transistor Q1 301 the current in the collector terminal of transistor Q2 302 is M times larger than the current in the collector terminal of transistor Q1 301. Thus, the mean current propagating through

the load resistor, R1 331 from the second ratio output port 306b, is  $M^*N^*I_{in}$  when there is no RF modulation provided to the circuit via the RF input port 300c.

**[0028]** Optionally, when the circuit components that comprise the wide ratio current mirror circuit 300 are integrated on a semiconductor substrate and the process offers particularly high NPN beta for the transistors Q1 301 and Q2 302, it may be advantageous to add a forward biased diode (not shown) from the node formed at the junction of resistors R2 332, R3 333 and R4 334 down to the second supply voltage port 300b in order to provide stability. This is implemented where the overall ratio of current output at the second current ratio output port 306b to current sunked ( $I_{in}$ ) from current sink 321 is less than a DC current gain of the bipolar transistors Q1 301 and Q2 302. Under this condition the current flowing in the drain terminal of FET M3 313 is less than the sunked current  $I_{in}$  and the pole splitting action of C1 341 does not occur. The addition of the diode increases the current draw from the drain terminal of FET M3 313. This addition of the forward biased diode is optionally implemented in all embodiments of the invention in order to reduce the impedance at the junction of resistors R2 332, R3 333 and R4 334, thereby improving the effectiveness of the pole splitting of capacitor C1 341.

**[0029]** For example, the wide ratio current mirror circuit 300 shown in FIG. 3 is for being used in conjunction with a PA output stage in a DECT, which is a digital wireless technology known to those of skill in the art.

**[0030]** Further optionally, the PNP transistors are used in order to replace FETs M1 311 and M2 312 and optionally FET M3 313. However, this is less desirable, especially for FET M3 313, because bipolar transistors, unlike FETs, have finite current gain.

**[0031]** Advantageously, the first and second embodiments of the invention provide significant improvements in precision in output current for a low voltage PA without incurring an overhead of quiescent current. Furthermore, the second embodiment of the invention 300 utilizes the voltage swing reduction circuit in order to provide stability thereto. Additionally, the embodiments of the invention offer a wide ratio current mirror

circuit that provides an output current that is a multiple of already multiplied current, which is advantageous over that attainable in the prior art.

[0032] FIGs. 4a and 4b illustrates an implementation of a variation of the wide ratio current mirror circuit 200 for use with a differential RF input signal, in accordance with third 400 and fourth 450 embodiments of the invention. A first supply voltage port 400a is used for receiving a positive supply voltage, a second supply voltage port 400b is used for receiving a negative, or ground, supply voltage. Differential RF input ports, 400c and 400d, are disposed for receiving of a differential RF input signal.

[0033] A current mirror 405 is formed from FETs M1 411 and M2 412. The source terminals of the p channel FETs M1 411 and M2 412 are coupled to the first supply voltage port 400a. The gate terminals of the p channel FETs M1 411 and M2 412 are coupled together, coupled to the drain terminal of FET M1 411, and further coupled to the collector terminal of transistor Q1 401. A source terminal of FET M3 413 is coupled to the first supply voltage port 400a, with the gate terminal thereof coupled to the drain terminal of FET M2 412. A first current mirror port 405a is formed at the drain terminal of FET M2 412 and a second current mirror port 405b is formed at the drain terminal of FET M1 411.

[0034] Transistors Q1 401 and Q2 402 form a current ratioing circuit 406 circuit that includes a first portion disposed between the first current mirror port 405b and the second supply voltage port 400b and a second portion disposed between the first supply voltage port 400a and the second supply voltage port 400b, the second portion including a load current path that includes a load resistor 431. A current path is formed between the first supply voltage port 400a and the coupled base terminals of transistors Q1 401 and Q2 402. The current path includes the FET M3 413 and the resistor R3 433, with source and drain terminals disposed in series with resistor R3 433 along the current path from the first supply voltage port 400a to coupled base terminals of transistors Q1 401 and Q2 402. The gate terminal of FET M3 413 is coupled with the second current mirror port 405a. Transistors Q1 401 and Q2 402 are formed so as to provide a statistical match with

M times current ratio. The current flowing in the collector terminal of transistor Q2 402 is M times the current flowing in the collector terminal of transistor Q1 401.

**[0035]** A first current mirror 405 is formed from FETs M1 411 and M2 412. Preferably, the FETs M1 411 and M2 412 are positive channel FETs (PFETs). The source terminals of the PFETs M1 411 and M2 412 are coupled to the first supply voltage port 400a. The gate terminals of the p channel FETs M1 411 and M2 412 are coupled together, coupled to the drain terminal of FET M1 411, and further coupled to the collector terminal of transistor Q1 401. A source terminal of FET M3 413 is coupled to the first supply voltage input 400a, with the gate terminal thereof coupled to the drain terminal of FET M2 412. A second current mirror port 405a is formed at the drain terminal of FET M2 412 and a first current mirror port 405b is formed at the drain terminal of FET M1 411.

**[0036]** The current sink 421, for sinking of current  $I_{in}$ , is disposed between the second supply voltage port 400b and the second current mirror port 405a. A node formed between transistors Q1 401 and Q2 402 is coupled to the drain terminal of FET M3 413 via resistor R3 432 disposed in series. Source and drain terminals of FET M3 413 form a current path from the first supply voltage port 400a, via resistor R3 433, to coupled base terminals of transistors Q1 401 and Q2 402. Capacitor C1 441 is disposed between the gate and source terminals of FET M3 413 for providing loop stabilization for FET M3 413 and resistor R3 433 aids in a pole split for the circuits 400 and 450. Resistor R3 433 is used to isolate FET M3 413 from the coupled base terminals of transistors Q1 401 and Q2 402.

**[0037]** Miller feedback within the circuit is a result of the dominant pole formed by FET M3 413. A small change in current of FET M3 413 reflects back to gate through capacitor C1 441, where resistor R3 433 and capacitor C1 441 operate in conjunction as a voltage swing reduction circuit to reduce large voltage swings on the gate terminal of FET M3 413. Opposite to that which is provided by the prior art illustrated in FIG. 1a, which provides no stabilization correction.

[0038] In equilibrium the drain current of FET M2 412 balances the current  $I_{in}$  from the current sink 421 and the potential on the drain terminal of FET M2 412 biases the gate terminal of FET M3 413. This causes current flow in the drain terminal of M3 413, which drives the base terminals of transistors Q1 401 and Q2 402. The resultant collector current in transistor Q1 401 drives the first current mirror port 405b and causes current to flow in the drain terminal of FET M2 412. By making FET M1 411 N times wider than FET M2 412 the current in the collector terminal of transistor Q1 401 is N times larger than the current in the drain terminal of FET M2 412. By making transistor Q2 402 M times larger than transistor Q1 401 the current in the collector terminal of transistor Q2 402 is M times larger than the current in the collector terminal of Q1 401. Thus, the DC current propagating through the load, in the form of the differential amplifier 407, coupled between the second current ratio port 406b and the first supply voltage port 400a, is  $M*N*I_{in}$ , as shown. A second current source 422 is coupled to the base terminal of transistor Q2 402 and provides an offset current,  $I_{offset}$ , thereto.

[0039] The differential amplifier 407 comprises a differential bias port 407c coupled with the second current ratio output port 406b, a first bias port 407a, a second bias port 407b, and first and second RF signal input ports 400c and 400d in the form of differential RF input ports. A differential pair of seventh and sixth bipolar transistors Q3 403 and Q4 404, respectively, is disposed with coupled emitter terminals and coupled with the differential bias port 407c. First and second load resistors, R1 431 and R2 432, are coupled in series between the collector ports of the first and second bipolar transistors Q3 403 and Q4 404, respectively, and the first supply voltage port 400a. A first bias resistor R4 434 is disposed between the first bias port 407a and the base terminal of transistor Q4 404. A second bias resistor R5 435 is disposed between the second bias port 407b and the base terminal of transistor Q3 403. The first and second bias ports, 407a and 407b, are coupled to the drain terminal of FET M3 413. A second capacitor C2 442 couples the first RF input port 400c to the base terminal of transistor Q4 404. A third capacitor C3 443 couples the second RF input port 400d to the base terminal of transistor Q3 403.

[0040] Base terminal bias for transistors Q3 403 and Q4 404 is offset above the base terminal bias for transistor Q2 402 because of by the second current source 422 coupled to the base terminal of transistor Q2 402. Preferably transistor Q2 402 operates as close to saturation as possible in order to maximize the potential difference that is available to load, in the form of the differential amplifier 407.

[0041] In the third embodiment of the invention 400, the bipolar transistor devices, Q1 401 Q2 402 Q3 403 and Q4 404, are fabricated on a same semiconductor substrate with a similar construction and manufacturing process so that they have closely matching electrical characteristics. Thus, in an ideal situation, the base current (IbQ2) propagating into transistor Q2 402 matches the combined base current propagating into transistor Q3 403 (IbQ3) and into transistor Q4 404 (IbQ4).

[0042] The voltage drop (VdropR3) across resistor R3 433 is provided by equation (1):

$$V_{dropR3} = (IbQ1 + IbQ2 + Ioffset) * R3 \quad (1)$$

, where IbQ1 is the base current propagating into transistor Q1 401 and IbQ2 is the base current propagating into transistor Q2 402. The voltage drop across resistor R3 433 is also expressed as equation (2):

$$V_{dropR3} = (IbQ2(1+1/M) + Ioffset) * R3 \quad (2)$$

[0043] By selecting resistor  $R3 = R4(1+1/M)/2$ , the voltage drop across resistor R3 is matched to the voltage drops across resistors R4 434 or R5 435 due to the base currents IbQ3 and IbQ4. The voltage on the collector terminal of transistor Q2 402 is  $Ioffset * R3$ . In an actual implementation of the circuit 400, the Early voltage realized on the NPN transistors, 403 and 404, causes the base current propagating into transistors Q3 403 and Q4 404 to be slightly less than the base current propagating into transistor Q2 402. This difference is preferably corrected by a small reduction in the resistance of resistor R3 433.

[0044] Referring to FIG. 4b, a variant of the third embodiment 400 of the invention is shown as a fourth embodiment of the invention 450. In the fourth embodiment 450 the collector current of transistors 403 Q3 and 404 Q4 is preferably independent of the manufacturing process beta for the transistors and is preferably proportional to absolute temperature (PTAT). Additionally, a resistor R6 436 is disposed between the base terminals of transistors Q1 401 and Q2 402. This resistor R6 436 compensates for the process beta and sets the current in the collector terminals of transistors Q3 403 and Q4 404 independent of the beta. This type of implementation is preferable for use with low noise amplifier (LNA) circuits where a PTAT collector current gives a gain characteristic independent of temperature. In this embodiment, source and drain terminals of FET M3 413 form a current path from the first supply voltage port 400a, via resistor R3 433, to coupled base terminals of transistors Q1 401 and Q2 402.

[0045] In the third and fourth embodiments of the invention, 400 and 450, preferably resistor  $R3 = R4(1+1/M)/2$ , thus providing beta compensation. Preferably transistor 401 Q1 is a small device in relation to transistor 402 Q2, which is much larger. Transistor Q2 402 does not operate at 0V, thus the second current source 422 provides Ioffset to resistor R3 433 in order to elevate the potential of transistor Q2 402 to approximately 300-400mV above a potential of the second supply voltage port 400b. In order to not waste available voltage headroom, the second current source 422 preferably provides enough Ioffset to Q2 402 in order to facilitate operation thereof and no more. Preferably, the collector voltage of transistor Q2 402 is independent of supply voltage provided to the first supply voltage port 400a. Optionally, the second current source provides Ioffset independent of temperature. Advantageously, the third and fourth embodiments of the invention utilize the wide ratio current mirror 200, shown in FIG. 2, in order to provide precision bias to the load, in the form of the differential amplification stage 407.

[0046] For example, the circuits 400 and 450 shown in FIGs. 4a and 4b are for being used in conjunction with a differential PA output stage in a DECT, which is a digital wireless technology known to those of skill in the art.

**[0047]** Further optionally, the PNP transistors are used in order to replace FETs M1 211, 311, 411 and M2 212, 312, 412 and optionally FET M3 213, 313, 413. However, this is less desirable, especially for FET M3 213, 313, 413, because bipolar transistors, unlike FETs, have finite current gain.

**[0048]** Numerous other embodiments may be envisaged without departing from the spirit or scope of the invention.